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21 LEVEL HYBRID SINGLE T TYPE DOUBLE H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

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***Abstract*— Inverters are the power electronic circuits which transfers power from direct current source to alternating current load. It manages voltage, current and frequency of the signal. Inverter comprises of various applications like adaptable velocity AC motor drives, uninterruptible power supply, running appliances of AC used in automobile battery, etc. The simulation of 21 level multilevel inverter is taken out using MATLAB/Simulink and the simulated circuit model is discussed. The input DC voltage sources for inverter are assigned with the magnitudes 96V, 96V and 96V satisfying the ratio 3:3:3 for the frequency of 50 Hz and the results analyzed for resistive load and inductive load with fundamental switching pattern. The circuit is simulated with half height method and fundamental equal phase angle method and the THD is calculated and compared.**

***Keywords*— H-Bridge, Multilevel inverter, 21 level.**

I. INTRODUCTION

Inverters are the power electronic circuits which transfers power from direct current source to alternating current load. It manages voltage, current and frequency of the signal. Inverter comprises of various applications like adaptable velocity ac motor drives, uninterruptible power supply, running appliances of ac used in automobile battery, etc. On the specific device involved, the resulting AC frequency acquired is dependent. Inverters perform the reverse working of converters, which includes the usage according to the requirement. Dependency on the design of the particular device is important as voltage of input, output, frequency and total power operation are allied to implementation. Power is delivered through DC source and inverter does not process any power. The inverter is able to provide square waveform, modified sine waveform, pulsed sine waveform, pulse width modulated waveform or sine waveform and it all depends on the design of the circuit. The quasi-square wave and the square wave is produced by the common type of inverter. The clarity in sine wave measured by total harmonic distortion. For the power inverter device, the AC output frequency is generally alike as standard power line frequency.

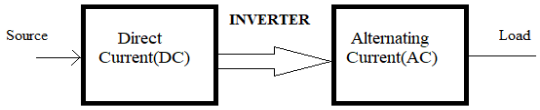

Fig. 1. Basic simplified illustration of Inverter.

Power electronics technology has reached significant stage of power semiconductor bias, transformers, pulse width modulation (PWM) ways, electrical machines, motor drives, advanced control, and simulation ways [1]. In this paper sinusoidal pulse width modulation for cascaded h- Ground multilevel inverter is performed. A comparison is made between the proposed inverter, classical CHB and some of the recent developed MLI topologies with respect to specified figure of graces, as well as the per unit power losses [2][3]. This module is can be used to produce a negative position without any fresh circuit similar as an H- ground which causes reduction of voltage stress on switches. The modular topology with other situations and new voltages can be obtained by cascade connection [4][5]. Distinct PWM approaches for inverter structure and the usage of H bridge cell to acquire high voltage level is performed. For the developed design it includes 4 H bridge MOSFETs based inverter, 4 distinct input sources, a microcontroller- based Arduino module, and isolating circuit [6][7]. The overall waveform of 21 level is designed by a 7-level inverter, with involvement of the updated strategy with not equal sources. Therefore, close sinusoidal waveform has been achieved with the same number of switches. For several techniques in level shifted PWM approach the THD differentiation for every level mentioned is done for modifying frequency 1KHz and 4KHz. Structures designed here are 7 level and 21 level, with reasonable cost and components. Both mentioned levels have cascaded with the another conventional one and enhanced to ‘n’ level. [8-10]. The module is a square combination of two back-to-back T-type inverters and some other switches. Square T-Type (ST-Type) Module produces 17 situations by 12 switches and four unstable DC sources (two 3VDC and two 1VDC). For two cascaded modules, simulation and experimental verifications are carried out on the proposed inverter topology for an R-L load. new topology for a single-phase cascaded H- Ground multilevel inverter (CHB MLI) with a focus to reduce the number of power switching bias in the path for the inflow of current [11-13].

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II. PROPOSED ALGORITHM

A. 21 level inverter topology

In this updated multilevel inverter, the configuration utilized is Hybrid single T-Type Double H-Bridge. The basic unit consist of 8 unidirectional switches and 2 bidirectional switches with 4 DC Voltage sources. 3Dc Voltage sources with magnitude of 3Vdc are connected on the LHS of the preferred basic unit. This 3 DC Voltage sources along with the 2 Bi directional switch S11 and S12 is from the T-Type section of the preferred basic unit. The T-Type section is administered at a High Voltage and the Low Frequency. the switches S2-S9 From 2 H-Bridge, i.e.,1 H-Bridge (H1) formed by S2, S3, S8 and S9 from the other H-Bridge with a Dc Voltage source with a Magnitude of VDC and Remaining switches S4-S7 From the Other H-Bridge(H2) with a DC Voltage source with a Magnitude of VDC H1 works at the low switching frequency and H2 Operates at the High switching Frequency. The load is connected between these 2 H-Bridges. figure 3.1. Depicts 21-level Single T-Type Double H-Bridge Multilevel Inverter.

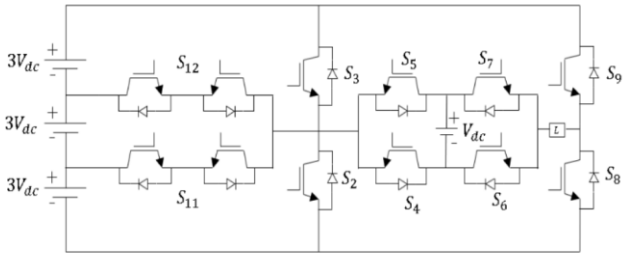

Fig. 2. 21 Level Inverter Topology.

This topology provides some more benefits like lower electromagnetic interference, improvement in the output waveform, and low THD. To perform the operation for this new topology, dc sources with different values and twelve switches is been provided to generate twenty-one level output. The modified topology has less complexity in design, cost, and lower switching losses because of the less switches in number. The THD amount in the output will be decreased as it successfully decreased the lower-level harmonics. The switches will be ON and OFF corresponding to the voltage level. The switching table shows the switches ON and OFF during each voltage level and the output voltage obtained during each stage.

Table 1: Operating table for the proposed 21 level multilevel inverter

Voltage levels	S 11	S 12	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9
0	0	0	1	0	1	0	1	0	1	0
+1V	0	0	1	0	1	0	0	1	1	0
+2V	1	0	0	0	0	1	1	0	1	0
+3V	1	0	0	0	0	1	0	1	1	0
+4V	1	0	0	0	1	0	0	1	1	0
+5V	0	1	0	0	0	1	1	0	1	0
+6V	0	1	0	0	0	1	0	1	1	0
+7V	0	1	0	0	1	0	0	1	1	0
+8V	0	0	0	1	0	1	1	0	1	0
+9V	0	0	0	1	0	1	0	1	1	0
+10V	0	0	0	1	1	0	0	1	1	0
0V	0	0	0	1	0	1	0	1	0	1
-1V	0	0	0	1	0	1	1	0	0	1
-2V	0	1	0	0	1	0	0	1	0	1
-3V	0	1	0	0	1	0	1	0	0	1
-4V	0	1	0	0	0	1	1	0	0	1
-5V	1	0	0	0	1	0	0	1	0	1
-6V	1	0	0	0	1	0	1	0	0	1
-7V	1	0	0	0	0	1	1	0	0	1
-8V	0	0	1	0	1	0	0	1	0	1
-9V	0	0	1	0	1	0	1	0	0	1
-10V	0	0	1	0	0	1	1	0	0	1

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Mode 1: To attain output voltage level as zero, the switches which are activated are S_2, S_4, S_6, S_8. And over the load the voltage will be nil.

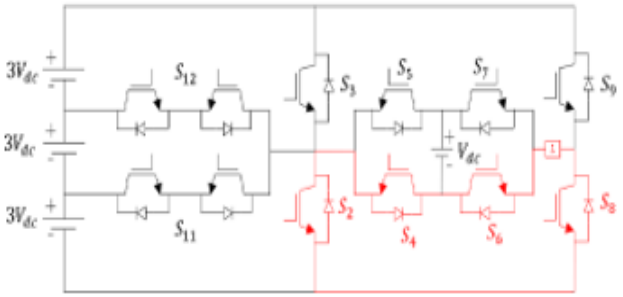

Fig: 3.1(i) Equivalent Circuit of Mode 1

Mode 2: For voltage level one in the output, the switches which are functioning are S_2, S_4, S_7, S_8 and over the load $1V_{dc}$ will be noticed.

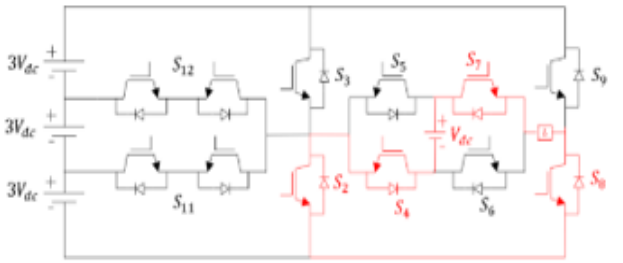

Fig: 3.1(ii) Equivalent Circuit of Mode 2

Mode 3: For voltage level two in the output, the switches which are activated are S_{11}, S_5 S_6, S_8 and over the load the $2V_{dc}$ is observed.

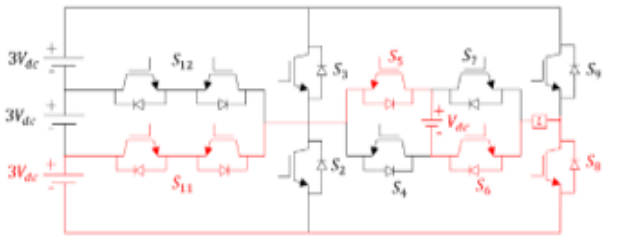

Fig: 3.1(iii) Equivalent Circuit of Mode 3

Mode 12: For the negative output voltage level one, the S3, S5, S7, S9 switches are activated and Output voltage $0V_{dc}$ is observed.

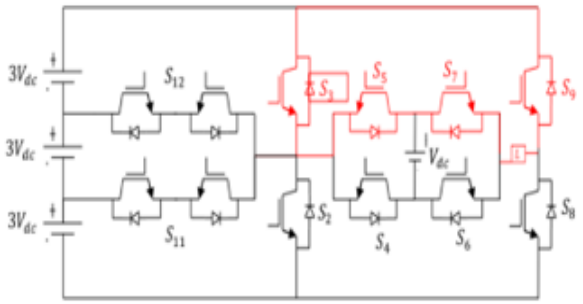

Fig: 3.1(xii) Equivalent Circuit of Mode 12

Mode 13: For the negative output voltage level two, the S3, S5, S6, S9, switches are activated and Output voltage $-1V_{dc}$ is observed.

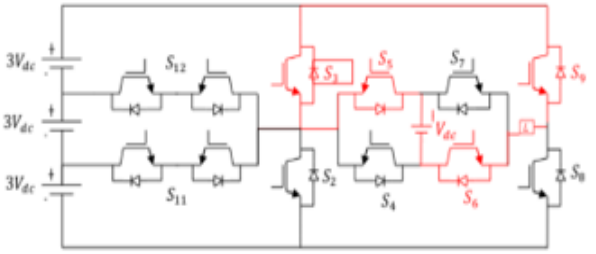

Fig: 3.1(xiii) Equivalent Circuit of Mode 13

Mode 14: For the negative output voltage level three, the S12, S4, S7, S9, switches are activated and Output voltage $-2V_{dc}$ is observed.

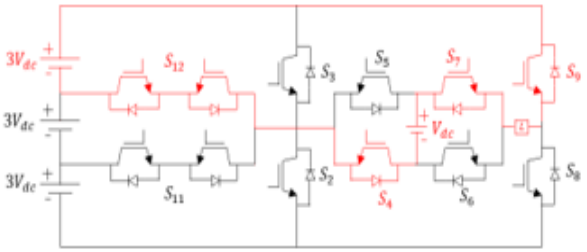

Fig: 3.1(xiv) Equivalent Circuit of Mode 14

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Mode 4: The switches S_{11}, S_5, S_7, S_8, are activated and the other switches are deactivated to get three in the output voltage level. The $3V_{dc}$ is observed.

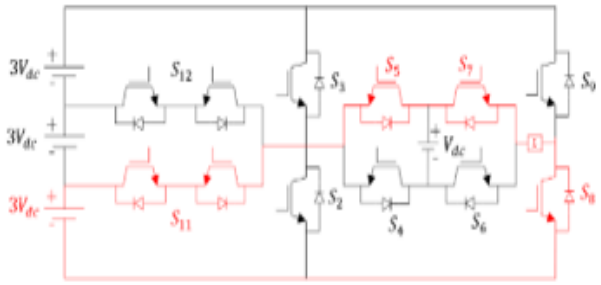

Fig: 3.1(vi) Equivalent Circuit of Mode 4

Mode 5: For output voltage level four, the activated switches are S_{11}, S_4, S_7, S_8, and remaining switches are not conducting. $4V_{dc}$ is observed.

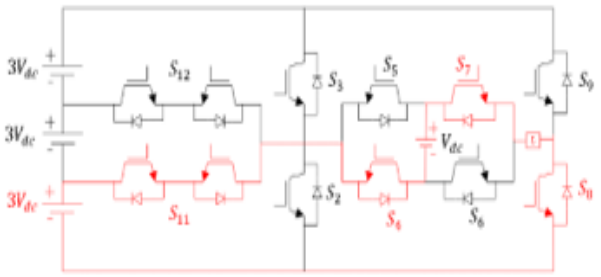

Fig: 3.1(v) Equivalent Circuit of Mode 5

Mode 6: For output voltage level five, the activated switches are S12, S5, S6, S8, and the output voltage $5V_{dc}$ is observed.

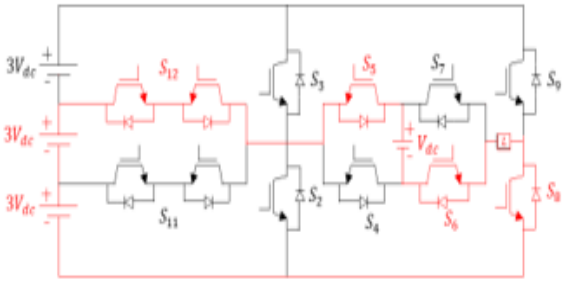

Fig: 3.1(vi) Equivalent Circuit of Mode 6

Mode 15: For the negative output voltage level four, the S12, S4, S6, S9, switches are conducting and remaining switches are deactivated. Output voltage $-3V_{dc}$ is observed.

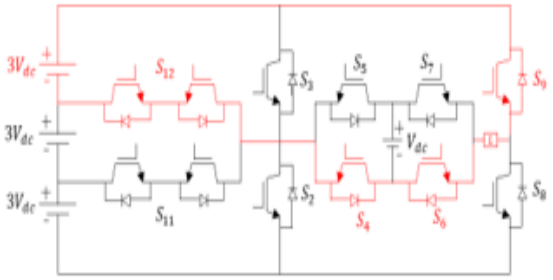

Fig: 3.1(xv) Equivalent Circuit of Mode 15

Mode 16: For negative output voltage level five, the S12, S5, S6, S9, switches are activated and the Output voltage $-4V_{dc}$ is observed.

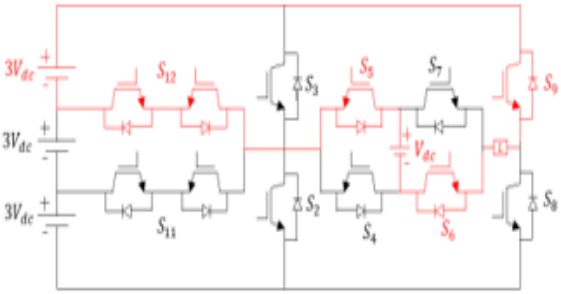

Fig: 3.1(xvi) Equivalent Circuit of Mode 16

Mode 17: For the negative output voltage level six, the S11, S4, S7, S9, switches are activated and the Output voltage $-5V_{dc}$ is observed.

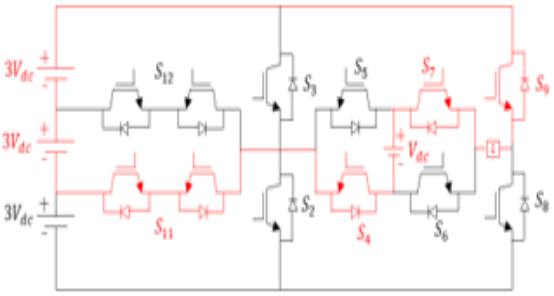

Fig: 3.1(xvii) Equivalent Circuit of Mode 17

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Mode 7: For the voltage level six, the switches which are activated are S12, S5, S7, S8, and the Output voltage $6V_{dc}$ is observed.

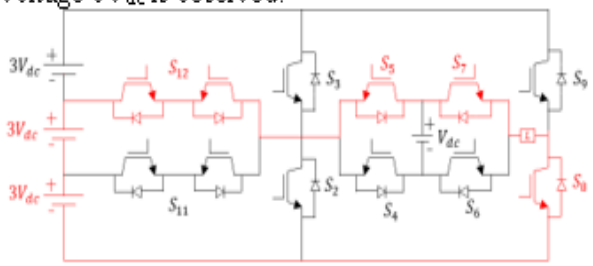

Fig: 3.1(vii) Equivalent Circuit of Mode 7

Mode 8: For the voltage level seven in the output, the activated switches are S12, S4, S7, S8, and the Output voltage $7V_{dc}$ is observed.

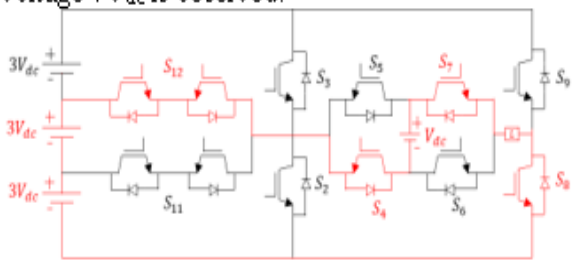

Fig: 3.1(viii) Equivalent Circuit of Mode 8

Mode 9: For the voltage level eight in the output, the switches which are activated S3, S5, S6, S8 and the Output voltage $8V_{dc}$ is observed.

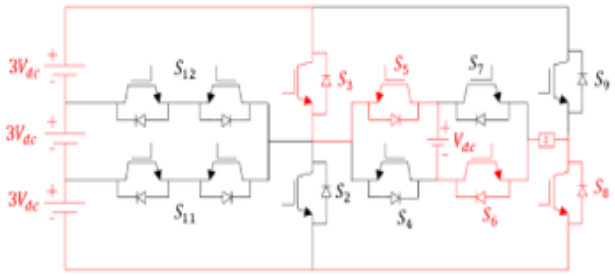

Fig: 3.1(ix) Equivalent Circuit of Mode 9

Mode 18: For the negative output voltage level seven, the S11, S4, S6, S9, switches are activated and the Output voltage $-6V_{dc}$ is observed.

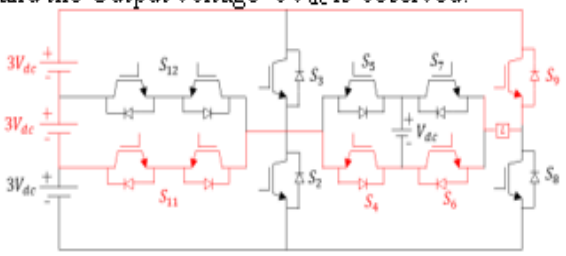

Fig: 3.1(xviii) Equivalent Circuit of Mode 18

Mode 19: For the negative output voltage level eight, the S11, S5, S6, S9, switches are activated and the Output voltage $-7V_{dc}$ is observed.

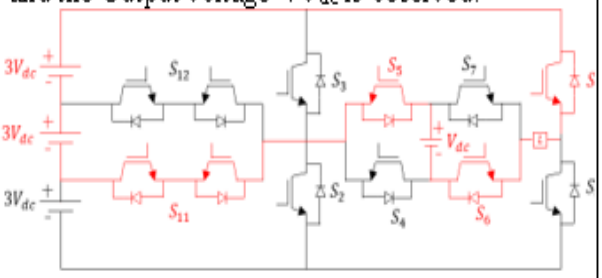

Fig: 3.1(xix) Equivalent Circuit of Mode 19

Mode 20: For the negative output voltage level nine, the S2, S5, S7, S9, switches are activated and remaining switches are deactivated. the Output voltage $-8V_{dc}$ is observed.

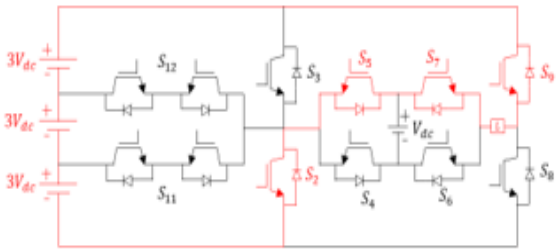

Fig: 3.1(xx) Equivalent Circuit of Mode 20

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Mode 10: For the voltage level nine in the output, the activated switches are S3, S5, S7, S8 and remaining switches are deactivated. The Output voltage $9V_{dc}$ is observed.

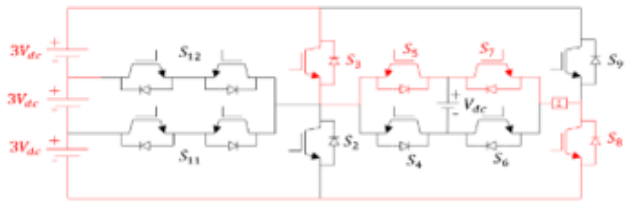

Fig: 3.1(x) Equivalent Circuit of Mode 10

Mode 21: For the negative output voltage level ten, the S2, S4, S6, S9, switches are activated and the Output voltage $-9V_{dc}$ is observed.

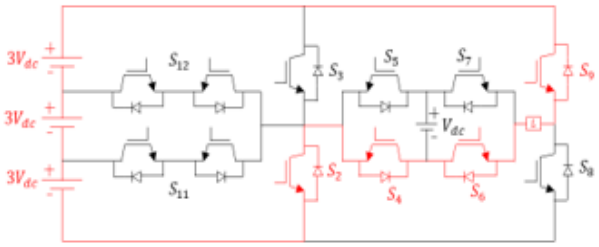

Fig: 3.1(xxi) Equivalent Circuit of Mode 21

Mode 11: For voltage level ten in the output, the activated switches are S3, S4, S7, S8, and the Output voltage $10V_{dc}$ is observed.

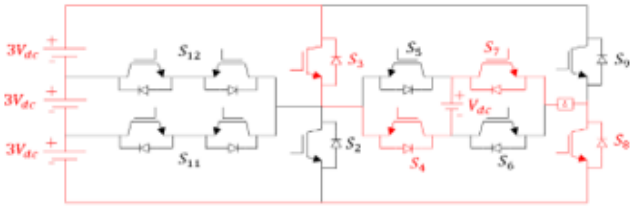

Fig: 3.1(xi) Equivalent Circuit of Mode 11

Mode 22: For the negative output voltage level ten, the S2, S5, S6, S9, switches are activated and the Output voltage $-10V_{dc}$ is observed.

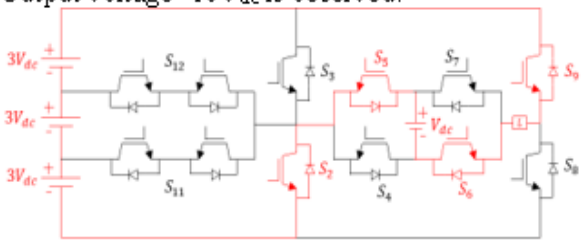

Fig: 3.1(xxii) Equivalent Circuit of Mode 22

III. SIMULATION RESULTS

A. POWER CIRCUIT DESIGN

The proposed inverter has 4 voltage sources Vdc, 3Vdc, 3Vdc, 3Vdc and their magnitudes are in ratio 1:3:3:3. The proposed multilevel inverter is simulated using MATLAB/Simulink and the results analyzed for resistive load and inductive load with fundamental switching pattern. The circuit is simulated with half height method and fundamental equal phase angle method and the THD is calculated and compared. From half height switching pattern we obtained least THD. The detailed comparison and analysis of each of the above simulation is done and control algorithms are presented.

Vdc: 3Vdc:3Vdc:3Vdc=230√2

Vrms = Vmax/ √2 (1)

Vo(rms)= Vdc+3Vdc+3Vdc+3Vdc =226.274Volts

The IGBT selected is NGTB10N60R2DT4G with current rating Io=10A, to obtain the approximate value of Vo(rms).

B. GATE CIRCUIT DESIGN:

For the generation of the 21-level voltage the generation of pulse is necessary with suitable pulse width to activate switches. There are different types of existing switching techniques. For this topology, to calculate switching angle two techniques are used i.e., Equal phase and Half height approach. Both switching techniques helps in the reduction of total harmonic distortion.

(I) Equal Phase approach

It is the method in which switching angles are dispersed averagely in the scale 0- π.

Analysis of switching angles in this method are represented using formula shown in equation

an=n*(180/L) (2)

Where n=1, 2, 3----------(L-1)/2

L defines the output voltage levels number. Switching angles will be averagely dispersed in the range 0-π.

(II) Half Height approach

As stated to the sine function a new method called half height method was established to find new switching angles. For one complete cycle, the total period is divided into four quadrants. The main switching angle estimation are obtained by evaluating the below equation

an=sin-1(2n-1)/(L-1) (3)

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Where n=1, 2, 3------- (L-1)/2

L=number of output voltage levels. Switching angle for 0-180 degree is considered as second quadrant for the output waveform, which is given by

$$a(L+1)/2 = \pi - a(L-1)/2,\ \pi - a(L-2)/2,\ \text{----------}\pi - a1 \quad (3)$$

For 180-270 degree, which is third quadrant switching angle calculated using the equation shown below

$$aL = \pi + a1,\ \pi + a2\text{----------}\pi + a(L-1)/2 \quad (4)$$

And for the fourth quadrant i.e., 270-360 degree as

$$a(3L-1)/2 = 2\pi - a(L-1)/2,\ 2\pi - a(L-2)/2,\ \text{---------}2\pi - a1 \quad (5)$$

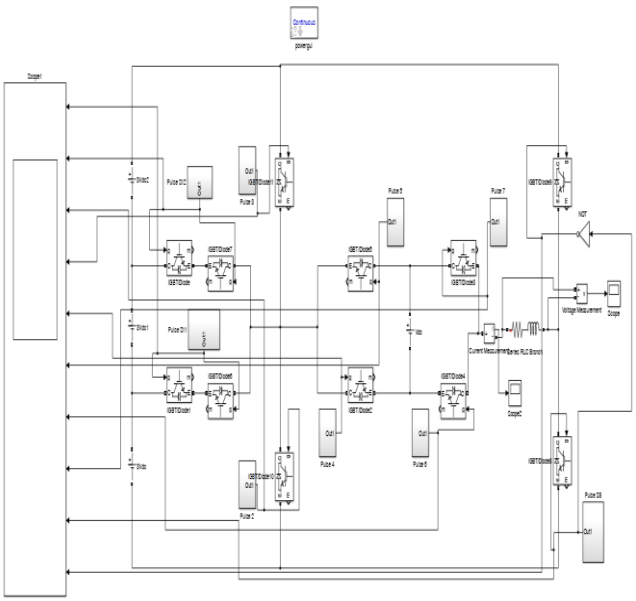

Fig. 4. MATLAB model of proposed 21 level inverters

The gating signals to the switches are given from pulse generators. For each level phase angle and pulse width is calculated from the MATLAB program written on script file and the calculated values are interrelated to pulse generators in the Simulink file. The IGBT switches with body diodes are used as semiconductor switching devices.

Equal Phase Method:
Resistive Load (R=22 Ω, Full load current IL=10A)

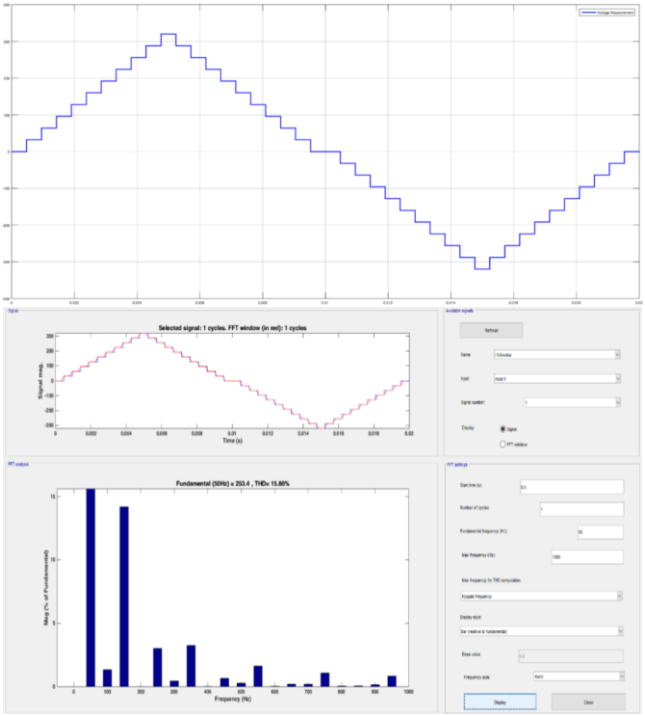

Fig. 5. (i) Output voltage waveform for resistive load R=22 Ω and full load current IL=10 A (ii) THD analysis of output voltage waveform using equal phase method

Inductive Load (R=21Ω, L=0.02087H and Full load current IL=10A)

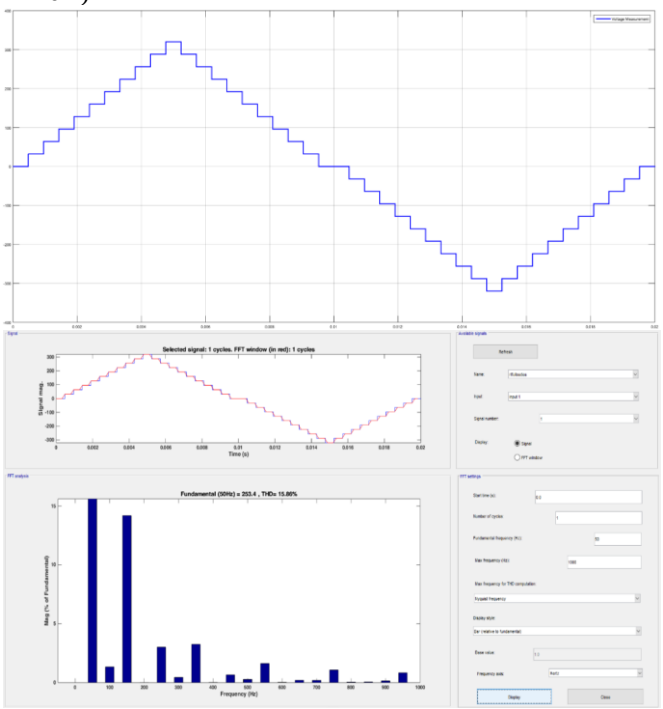

Fig. 6. (i) Vout waveform for inductive load with R=21 Ω , L=0.02087 H and full load current IL=10 A (ii) THD analysis of Vout waveform using equal phase method

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These are the output voltage and the output current waveform obtained for different load current along with the THD analysis window. The below table represents the voltage THD and the current THD for different loads.

Table 2: THD obtained using Equal phase method for resistive load

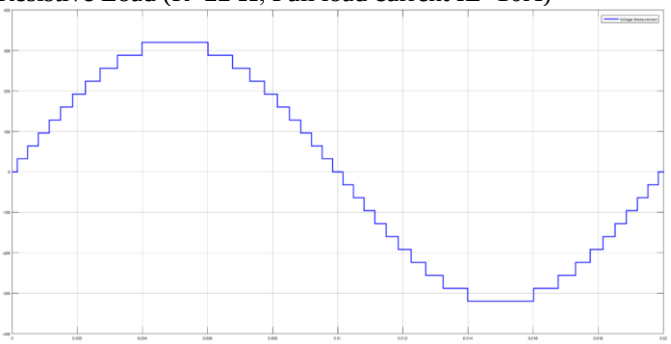
	R Value (in Ohms)	V_O (in Volts)	I (in Amperes)	V_O THD (in %)	I_O THD (in %)
Full Load	22	226	10	15.86	15.86
Half Load	45	226	5	15.86	15.86
Quarter load	90	226	2.5	15.86	15.86
No Load	450	226	0.5	15.86	15.86

Table 3: THD obtained using Equal phase method for inductive load

	R Value (in Ohms)	L value (in henry)	V_O (in Volts)	I (in Amperes)	V_O THD (in %)	I_O THD (in %)
Full Load	22	0.02087	226	10	15.86	12.47
Half Load	45	0.04222	226	5	15.86	15.86
Quarter load	90	0.12487	226	2.5	16.74	12.47
No Load	450	0.4228	226	0.5	16.74	12.49

Half Height Method:
In this method, for one complete cycle the total period is divided into four quadrants. After the values added to the model the results are been obtained.

Resistive Load (R=22 Ω, Full load current IL=10A)



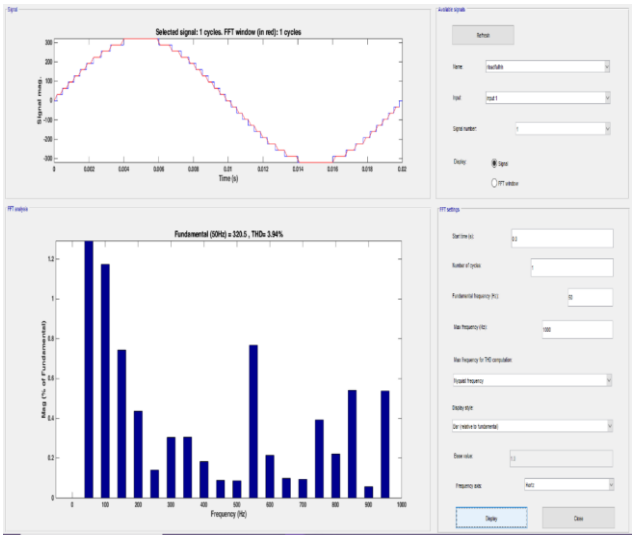


Fig. 7. (i) Output voltage waveform for resistive load R=22 Ω and full load current IL=10 A (ii) THD analysis of output voltage waveform using half height method

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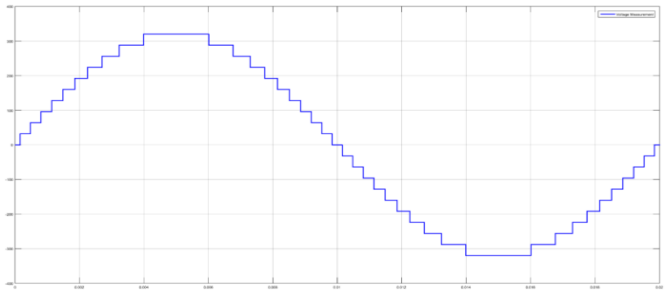
Inductive Load (R=21Ω, L=0.02087 H and full load current I_L=10 A)



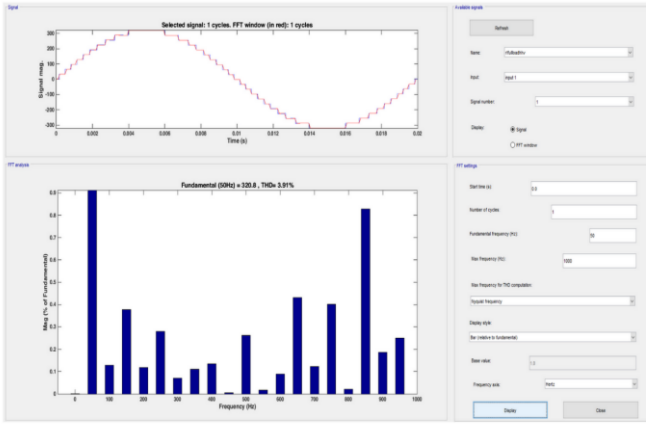


Fig. 8. (i) Vout waveform for inductive load with R=21 Ω, L=0.02087 H and full load current IL=10 A (ii) THD analysis of Vout waveform using half height method

Table 4: THD obtained using Half Height method for resistive load

	R Value (in Ohms)	V_O (in Volts)	I (in Amperes)	V_O THD (in %)	I_O THD (in %)
Full Load	22	226	10	3.94	3.94
Half Load	45	226	5	3.94	3.94
Quarter load	90	226	2.5	3.94	3.94
No Load	450	226	0.5	3.94	3.94

Table 5: THD obtained using Half height method for inductive load

	R Value (in Ohms)	L value (in henry)	V_O (in Volts)	I (in Amperes)	V_O THD (in %)	I_O THD (in %)
Full Load	22	0.02087	226	10	3.91	5.95
Half Load	45	0.04222	226	5	3.87	5.87
Quarter load	90	0.12487	226	2.5	3.92	1.68
No Load	450	0.4228	226	0.5	3.93	5.87

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Using equal phase method, the % variation of THD has a drastic change with the change in inductive load between 43mH to 450mH, where as in half height method there is very slight change variation of %THD with the change in inductive load.

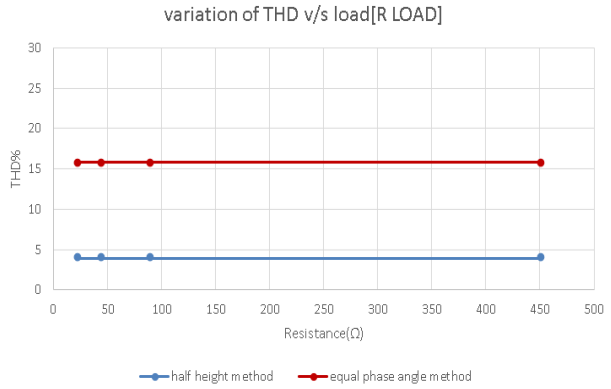

Fig. 9. Variation of THD with Resistive load

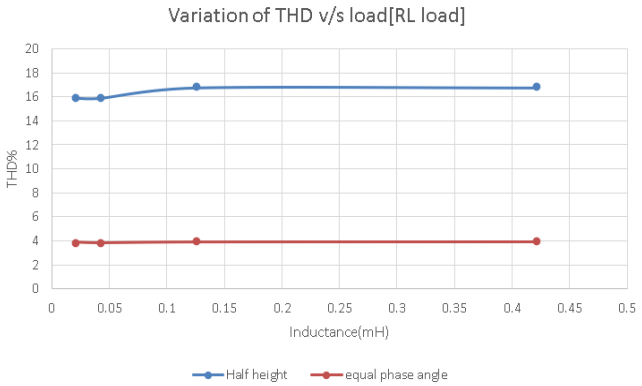

Fig. 10. Variation of THD with Inductive load

IV. CONCLUSION

The simulation of 21 level multilevel inverter is taken out using MATLAB/Simulink and the simulated circuit model is discussed. The input DC voltage sources for inverter are assigned with the magnitudes 96V, 96V and 96V satisfying the ratio 3:3:3 for the frequency of 50 Hz. The simulated Vout waveform for different loads by Equal phase method and half height method is obtained. The simulated Vout waveform for different loads by EP method and the THD analysis by EP method is observed. Output voltage waveform and the respective THD analysis Half height method is also observed respectively. The simulation is done by employing two distinct approaches. THD obtained by performing these two methods are 15.86% for equal phase approach and 3.90% for half height approach. Here overall results are accomplished with the help of MATLAB Simulink simulations.

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